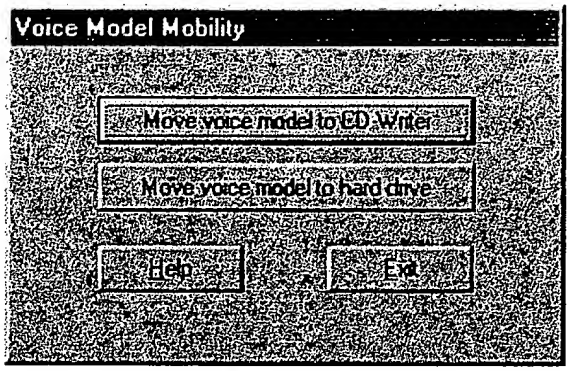


Figure 1

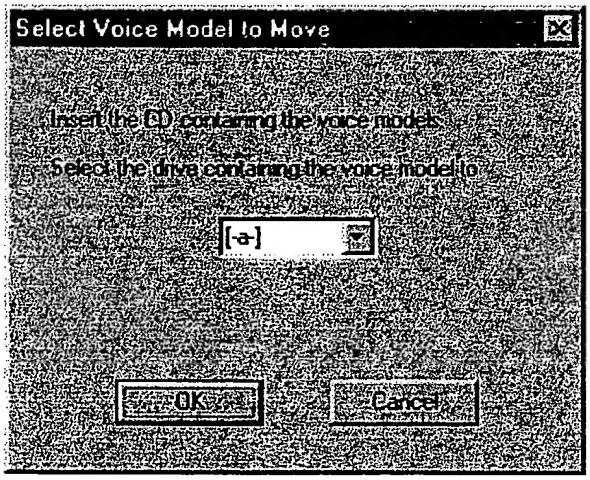
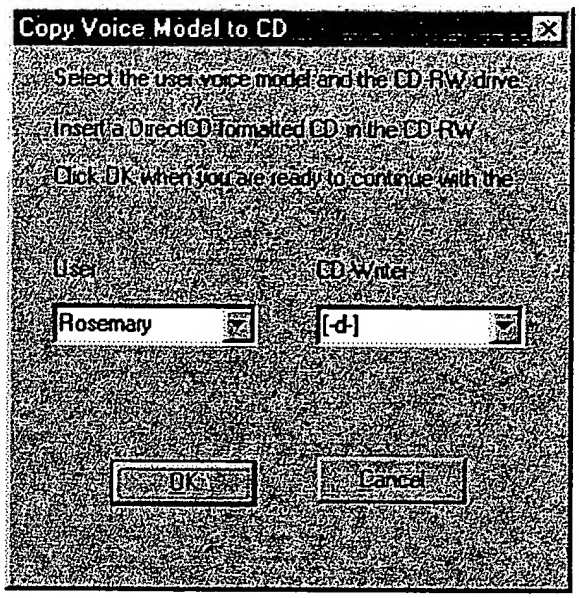


Figure 2



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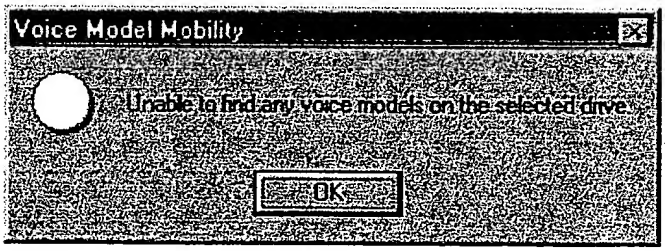

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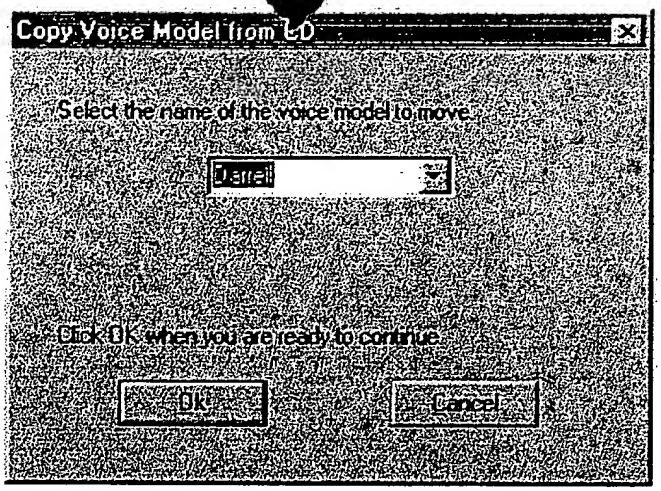


Figure 5

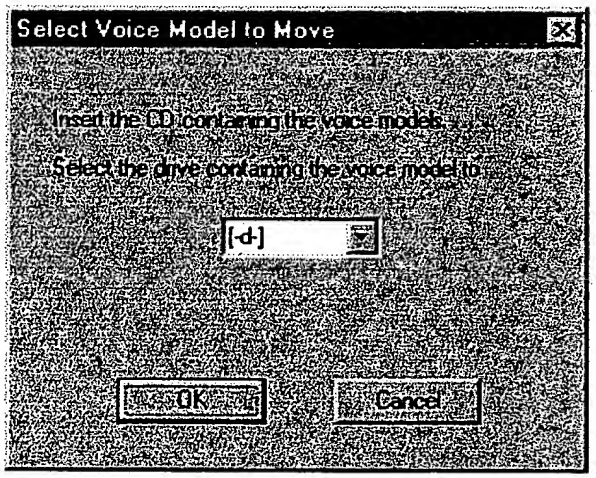
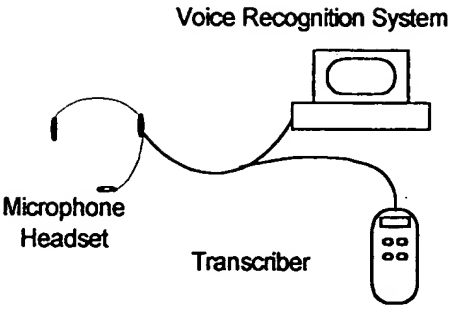


Figure 6



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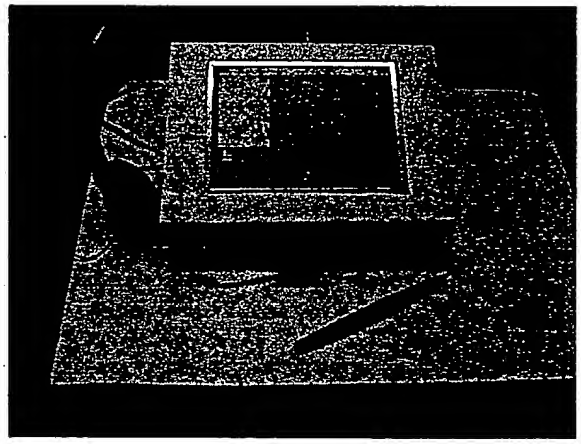


Figure 8

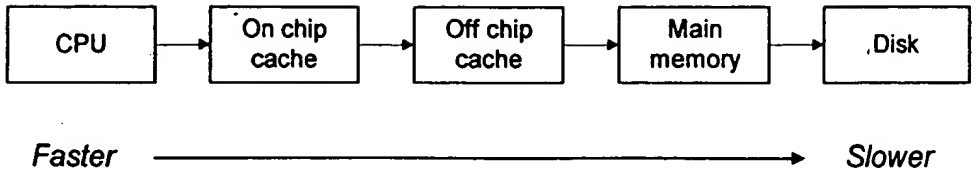
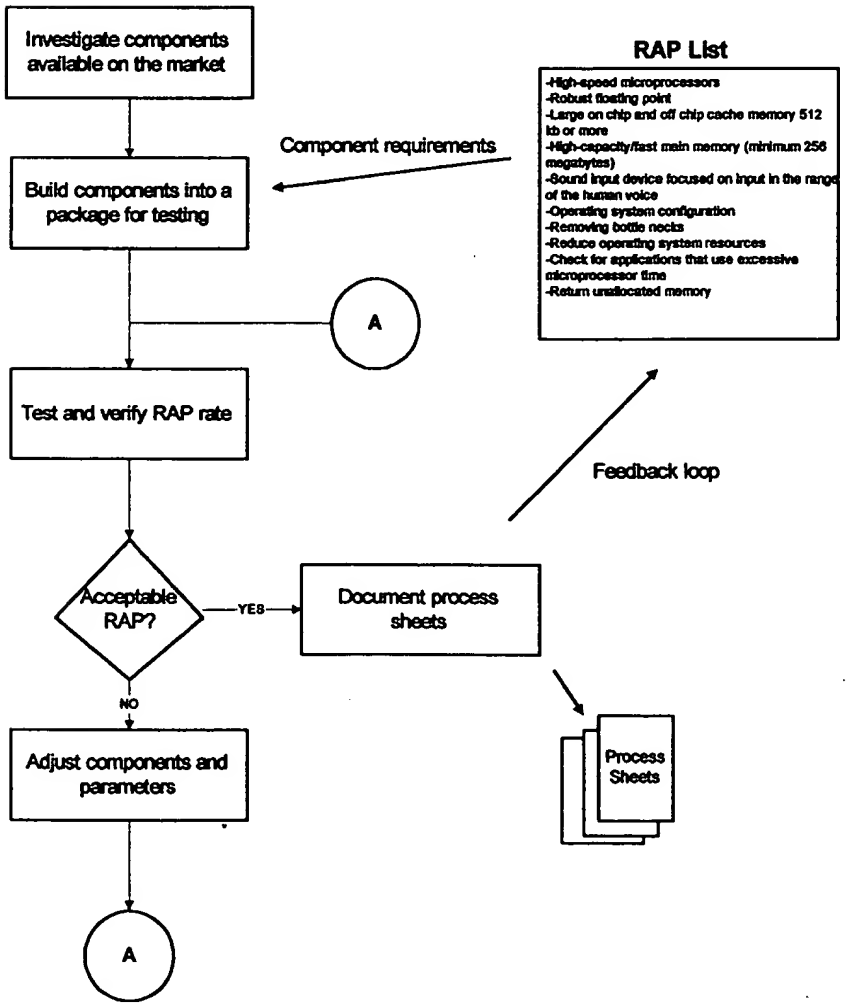


Figure 9

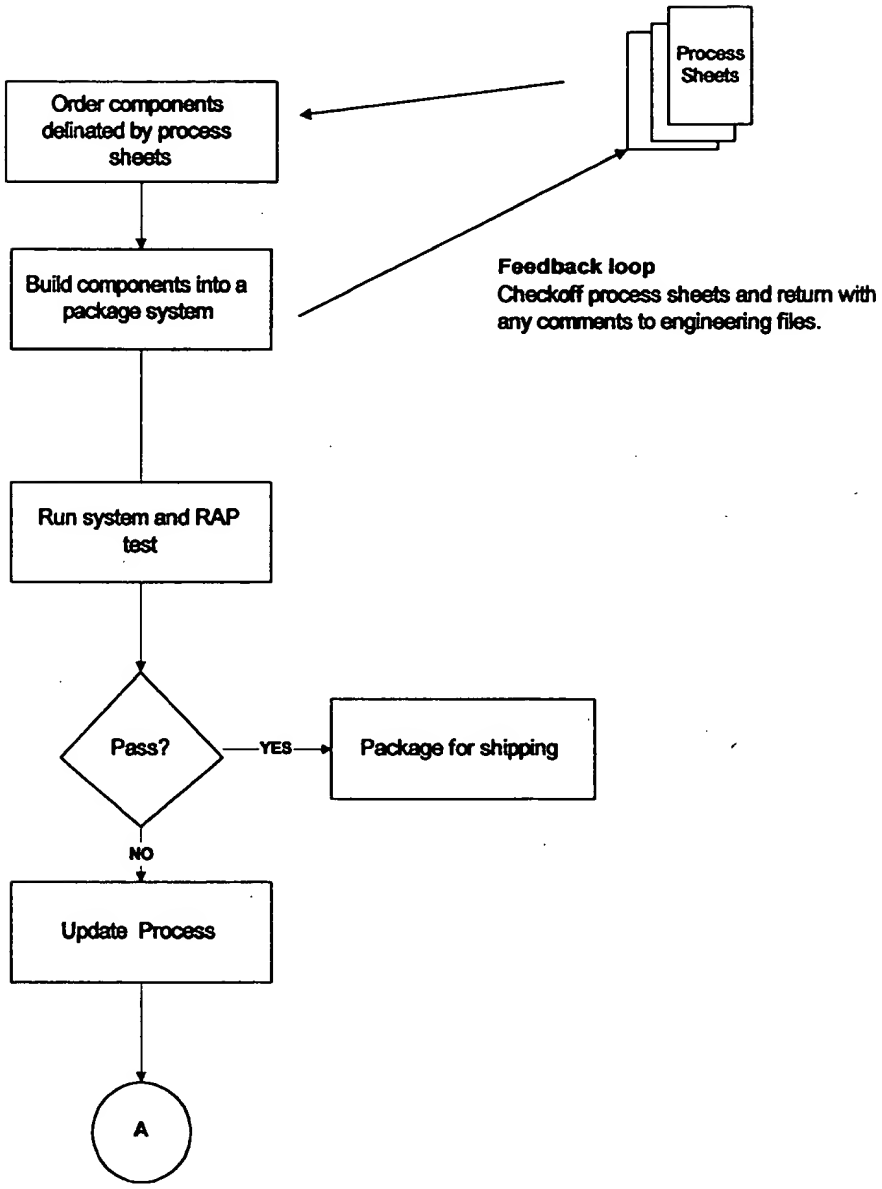
Development Process For LVVR



PROCESS 1

Darrell A. Poirier
006-110-300

Manufacture Process For LVVR



PROCESS 2

TABLE 1

Bios Setup B8-19-1999

Y	BIOS FEATURES	COMMENTS
	boot virus disabled	
	CPU level one cash enable	
	CPU level to cash enable	
	CPU level to cash ECC enabled	
	BIOS update enabled	
	turbo mode disabled	
	quick power on self test enabled	
	boot floppy disabled	
	who sequence = 8, C	
	IDE first	
	Floppy access control read/write	
	IDE HDD block mode sectors disabled	
	smart disabled	
	PS/2 auto	
	OS/2 on-board memory disabled	
	PCI/VGA palettes snoop disabled	
	video ROM shadow	
	Boot of number lock off	
	Defaults on the rest	
	CHIP SET FEATURES	
	SDRAM by SPD	
	SDRAM MA wait state = normal	
	snoop ahead: enabled	
	host bus fast data recovery: disabled	
	16-bit I/0 rec time: 4 bus clock	
	8-bit I/0 rec time: 8 bus clock	
	graphics aperture size: 64 MB	
	video memory cache mode: UC	
	memory hole at 15 m -- 16 m: disabled	
	on-board floppy: enabled	
	on-board floppy drive swap: disabled	
	on-board serial 1:3F8/IRQ 4	
	on-board serial 2:2F8/IRQ3	
	on-board parallel: 378/IRQ 7	
	ECP DMA: disabled	
	UART infrared: disabled	